ONBOARD HIGH DATA RATE SIGNAL PROCESSING AND STORAGE

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HISTORY

THE NEED TO INCREASE THE INFORMATION RETURN FROM SPACE-BORNE IMAGING SYSTEMS HAS GROWN DRAMATICALLY DURING THE PAST DECADE. THE GROWTH IN THE USE OF MULTISPECTRAL DATA HAS RESULTED IN THE NEED FOR GREATER SPATIAL RESOLUTION AND SPECTRAL COVERAGE. INCREASES IN RESOLUTION, FIELD OF VIEW AND NUMBER OF SPECTRAL BANDS HAVE ALL POINTED IN THE SAME DIRECTION...TOWARD INCREASED DATA RATES AND HIGHER BANDWIDTH REQUIREMENTS. FURTHERMORE, THE DATA RATE IMPLIED BY THESE IMPROVED PERFORMANCE CHARACTERISTICS CAN BE EXPECTED TO GROW MORE RAPIDLY THAN SPACECRAFT TELECOMMUNICATIONS CAPABILITIES. ALTHOUGH THE TELECOMMUNICATIONS CAPABILITY PLANNED THROUGH THE 1980S IS RELATIVELY LARGE, FEASIBILITY STUDIES ON SOLID STATE MULTISPECTRAL IMAGING INSTRUMENTS IN SUPPORT OF LAND OBSERVING SYSTEMS, USING CHARGE COUPLED DEVICES (CCD) TECHNOLOGY, UNCOVER DATA RATES THAT EXCEED THE TELECOMMUNICATIONS CHANNEL CAPACITY. ONBOARD SIGNAL/DATA PROCESSING WILL PLAY A PIVOTAL ROLE IN SATISFYING THE NEED FOR MORE INFORMATION BY UTILIZING THE AVAILABLE COMMUNICATION CHANNEL AT HIGHER EFFICIENCY.

THE OBJECTIVE OF THIS PROGRAM IS TO ADVANCE THE STATE-OF-THE-ART IN ONBOARD IMAGE DATA PROCESSING AND STORAGE THROUGH THE USE OF ADVANCE GAAS INTEGRATED CIRCUIT TECHNOLOGY. AS GAAS INTEGRATED CIRCUIT TECHNOLOGY MATURES, IT WILL BE ADVANTAGEOUS FOR SMART SENSOR SIGNAL PROCESSING, WHERE THE HARDWARE REQUIREMENT IS HIGH DATA RATE PROCESSING, AT LOW POWER AND INCLUDING RADIATION TOLERANCE.

FUTURE PLANS

THE OBJECTIVE OF AN EXISTING CONTRACT WITH ROCKWELL INTERNATIONAL IS TO MANUFACTURE A MICROPROCESSOR CHIP SET USING GAAS. THIS CHIP SET, WHEN FUNCTIONING TOGETHER ON A SINGLE CIRCUIT BOARD, WILL PERFORM HIGH DATA RATE IMAGE PROCESSING ALGORITHMS. THE INITIAL CHIP SET WOULD CONSIST OF FOUR DEVICE TYPES WITH THE ABILITY TO ADD FAMILY PARTS AS FUTURE SYSTEM DEMANDS REQUIRE. THE DEVICE TYPES WOULD INCLUDE: CONTROL SEQUENCER WITH ROM, 8 BIT SLICE GENERAL PROCESSOR, I/O AND INTERRUPT CONTROLLER, AND A GENERAL PURPOSE RAM. THIS CHIP SET USING GAAS TECHNOLOGY WOULD PRODUCE A FUNCTIONAL COMPUTER SYSTEM OPERATING WITH A 5 NANOSECOND MICROCYCLE TIME. IN 1985, THE CHIP SET ARCHITECTURE WILL BE DEFINED, AND THE CHIP

SET CRITICAL SPEED PATH ANALYZED TO ATTAIN A SYSTEM CLOCK RATE OF NO LESS THAN 200 MHZ. FOLLOWING TASKS WILL INCLUDE CHIP SET DESIGN, LAYOUT AND FABRICATION. FINALLY, THE CHIP SET WILL BE INTEGRATED ONTO A SINGLE CIRCUIT BOARD WITH THE CONTROL SEQUENCER, ROM MASK PROGRAMMED TO PERFORM AN IMAGING PROCESSING FUNCTION. WHEN CONFIGURING TWO 8-BIT SLICES OF THE GENERAL PROCESSOR, THE CHIP SET ARCHITECTURE WILL DEMONSTRATE EMULATION OF MIL-STD-1750A INSTRUCTION SET.

506-58-16

ONBOARD HIGH DATA RATE SIGNAL PROCESSING AND STORAGE

I. TECHNICAL OBJECTIVES

ADVANCE THE STATE-OF-THE-ART IN ONBOARD IMAGE SIGNAL PROCESSING AND STORAGE THROUGH THE USE OF ADVANCED GALLIUM ARSENIDE (GaAs) INTEGRATED CIRCUIT TECHNOLOGY.

II. TECHNICAL APPROACH

DESIGN, DEVELOP AND FABRICATE AN 8-BIT SLICE GaAs GENERAL PROCESSOR CHIP SET CAPABLE OF PERFORMING HIGH DATA RATE IMAGE PROCESSING ALGORITHMS. THE BIT SLICES CAN BE CASCADED TO PROVIDE DATA BUS WIDTH OF 8 BIT MULTIPLES (8, 16, 24, 32, 40). WHEN CONFIGURING TWO 8 BIT SLICES, THE CHIP SET ARCHITECTURE WILL DEMONSTRATE EMULATION OF MIL-STD-1750A INSTRUCTION SET.

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REAL TIME PROCESSING OF IMAGING ARRAYS

RELATIONSHIP BETWEEN SPATIAL RESOLUTION AND DATA RATE FOR ONE SPECTRAL BAND

ASSUMING 185K FOV AND AN EARTH VIEWING ALTITUDE OF 700KM

	IFOV (M)	# DET. PER FOV	INTEG. TIME (DWELL) (MSEC.)	PIXEL RATE	PIXEL PERIOD (MICRO SEC.)	SERIAL DATA RATE PER SPECTRAL BAND (B/SEC.)
	120	1542	17.7	87KPPS	11.5	695.7 K
MSS	80	2313	11.8	196K	5.1	1.57M
	60	3083	8.9	347.7K	2.9	2.78M
	40	4625	5.9	782.4K	1.3	6.26M
TM	30	6167	4.4	1.39MPPS	0.72	11.13M
	20	9250	2.9	3.13M	0.32	25.0 M
	15	12334	2.2	5.56M	0.179	44.5 M
ALOS/MLA	10	18500	1.47	12.5M	0.080	100.0 M

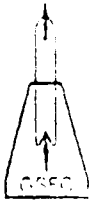
NASA RELATED R&D EFFORTS

* LASER COMMUNICATION (506-58-26)
  - CLOCK RECOVERY CIRCUITRY
  - MATCH FILTER
  - DATA DETECTOR AND MODULATOR

* RESEARCH OPTICAL SENSOR (666-51-70)
  - PIXEL AVERAGING
  - OFFSET SUBTRACTION
  - GAIN CORRECTION

* 150 MB/S REED-SOLOMON ENCODER/DECODER (310-20-46)
  - MULTIPLEXER/DEMULTIPLEXER

* COMPUTER VISION (488-32-02)
  - OFFSET SUBTRACTION/GAIN CORRECTION
  - SUN SHADE CORRECTION
  - CONTRAST ENHANCEMENT



WHY GaAs INTEGRATED CIRCUITS?

HIGH SPEED	100-200 PSEC GATE DELAYS
LOW POWER	0.5-2 MWATTS/GATE
RADIATION HARD	50 MRADS TOTAL DOSE
WIDE TEMPERATURE RANGE	-200°C TO 200°C

ADAPTIVE PROGRAMMABLE PROCESSOR CHIP SET

8-BIT SLICE GENERAL PROCESSOR UNIT

CONTROL SEQUENCER AND ROM

GENERAL PURPOSE ROM/RAM

I/O AND INTERRUPT CONTROLLER

GATE ARRAY

Rockwell International

PERFORMANCE GOALS
ADAPTIVE PROGRAMMABLE PROCESSOR

CLOCK RATE:	200 MILLION CLOCKS PER SECOND
ADD TIME:	5 nsecs
8 x 8 MULTIPLY TIME:	25 nsecs

THROUGHPUT (PERFORMING NON-UNIFORM QUANTIZER): 150 MIPS

PROGRAM HARDWARE DELIVERABLES

* THREE ADAPTIVE PROGRAMMABLE PROCESSING BOARDS

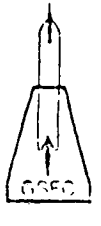
  ONE BOARD CONTAINING GATE ARRAY #1 AND ONE 8 BIT SLICE GENERAL PROCESSOR WHICH WILL PERFORM AN IMAGE DATA COMPRESSION ALGORITHM

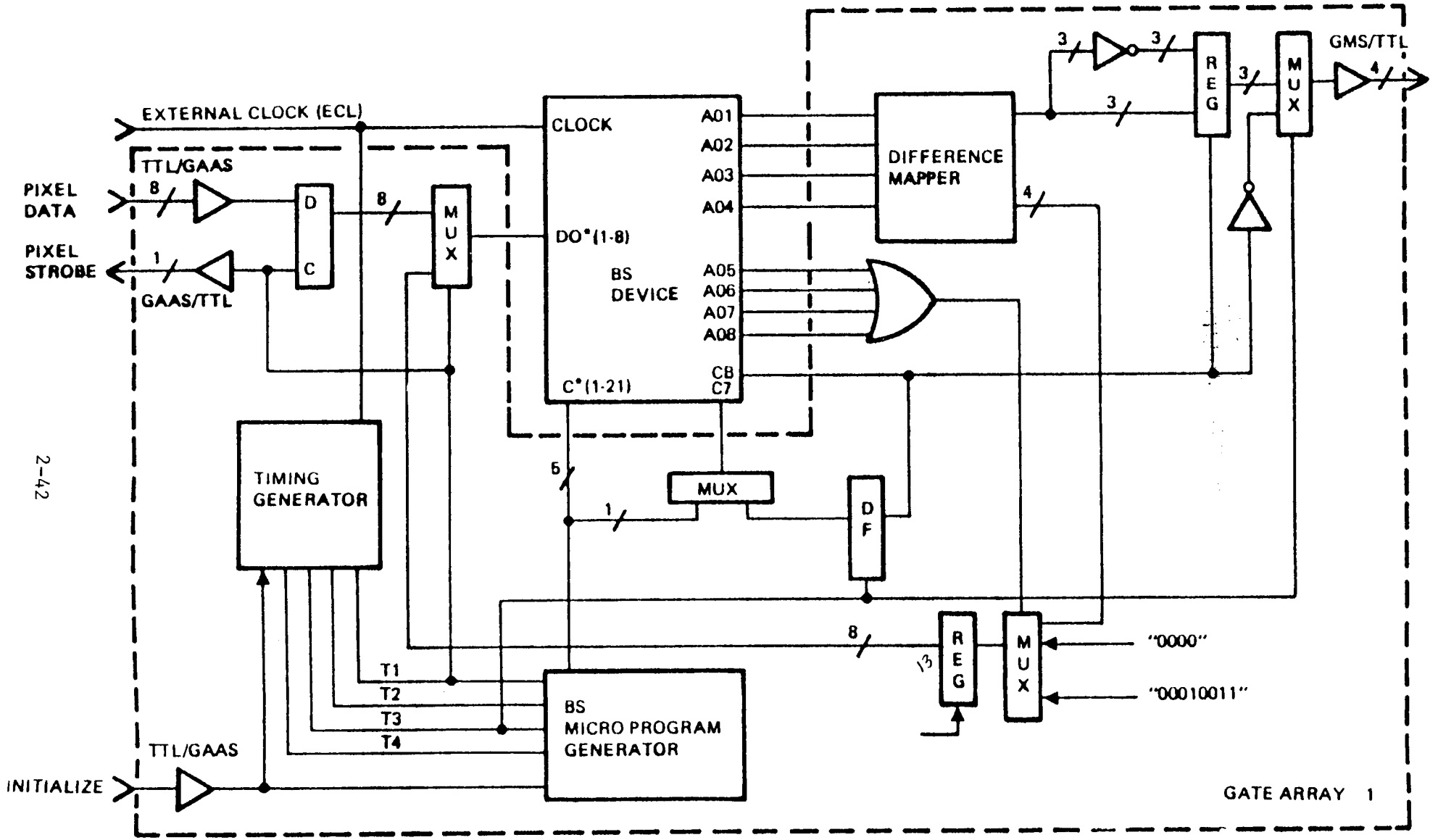
  TWO BOARDS EACH WILL CONTAIN:
  - TWO 8 BIT SLICE GENERAL PROCESSORS
  - ONE CONTROL SEQUENCER WITH AN INTERAL ROM (32K)
  - TWO GENERAL RAM (128x8)
  - TWO GATE ARRAYS FOR I/O AND INTERRUPT CONTROLLER

  AND CONFIGURED TO EMULATE THE 1750A INSTRUCTION SET.

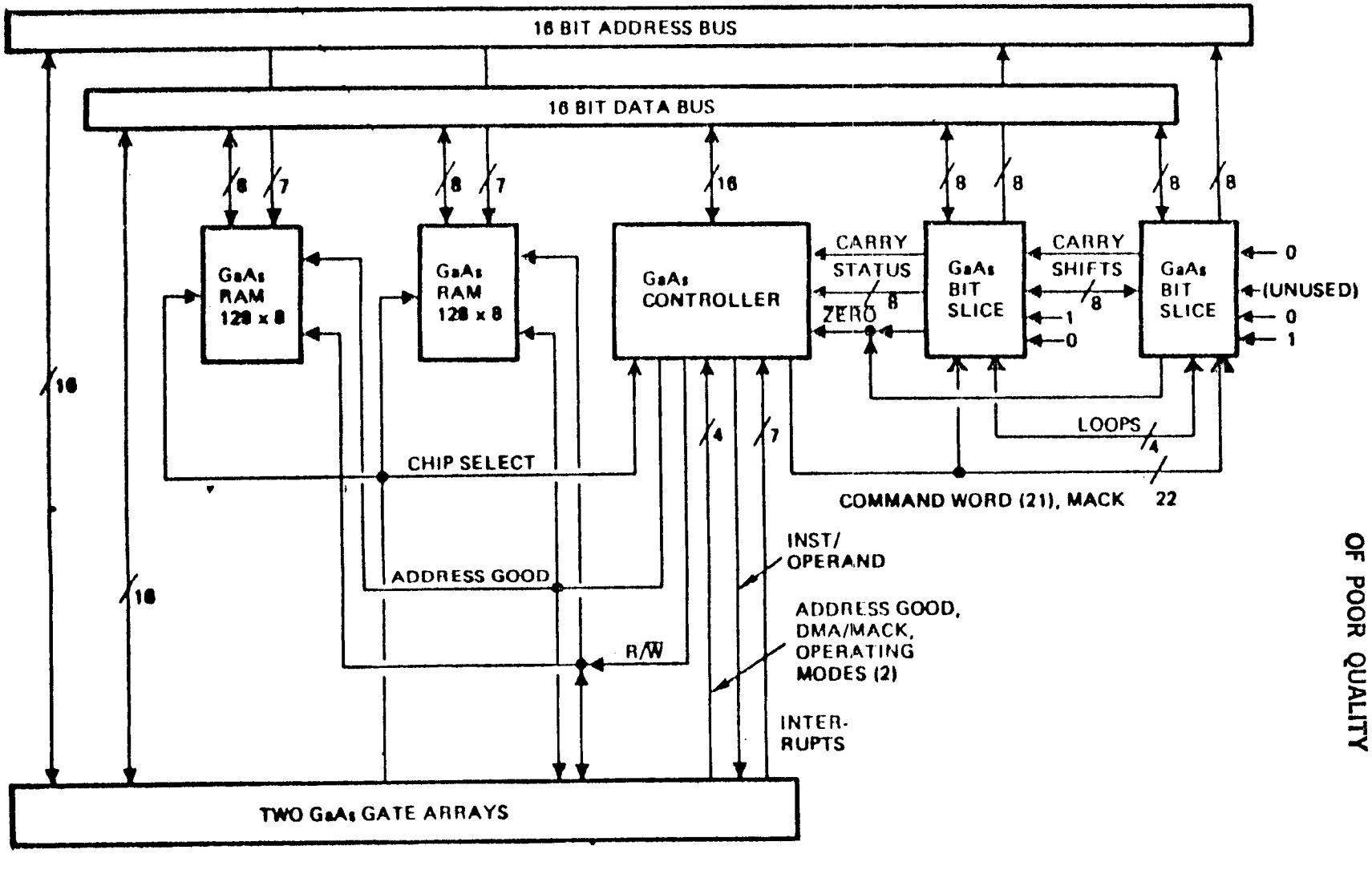
* SOFTWARE FOR THE FOLLOWING SIGNAL PROCESSING ALGORITHMS

  DPCM NOW UNIFORM QUANTIZER
  RADIOMETRIC CORRECTION
  DIGITAL FILTER
  (ONE TO BE DETERMINED).





The Non-Linear Quantrer Block Diagram



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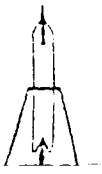
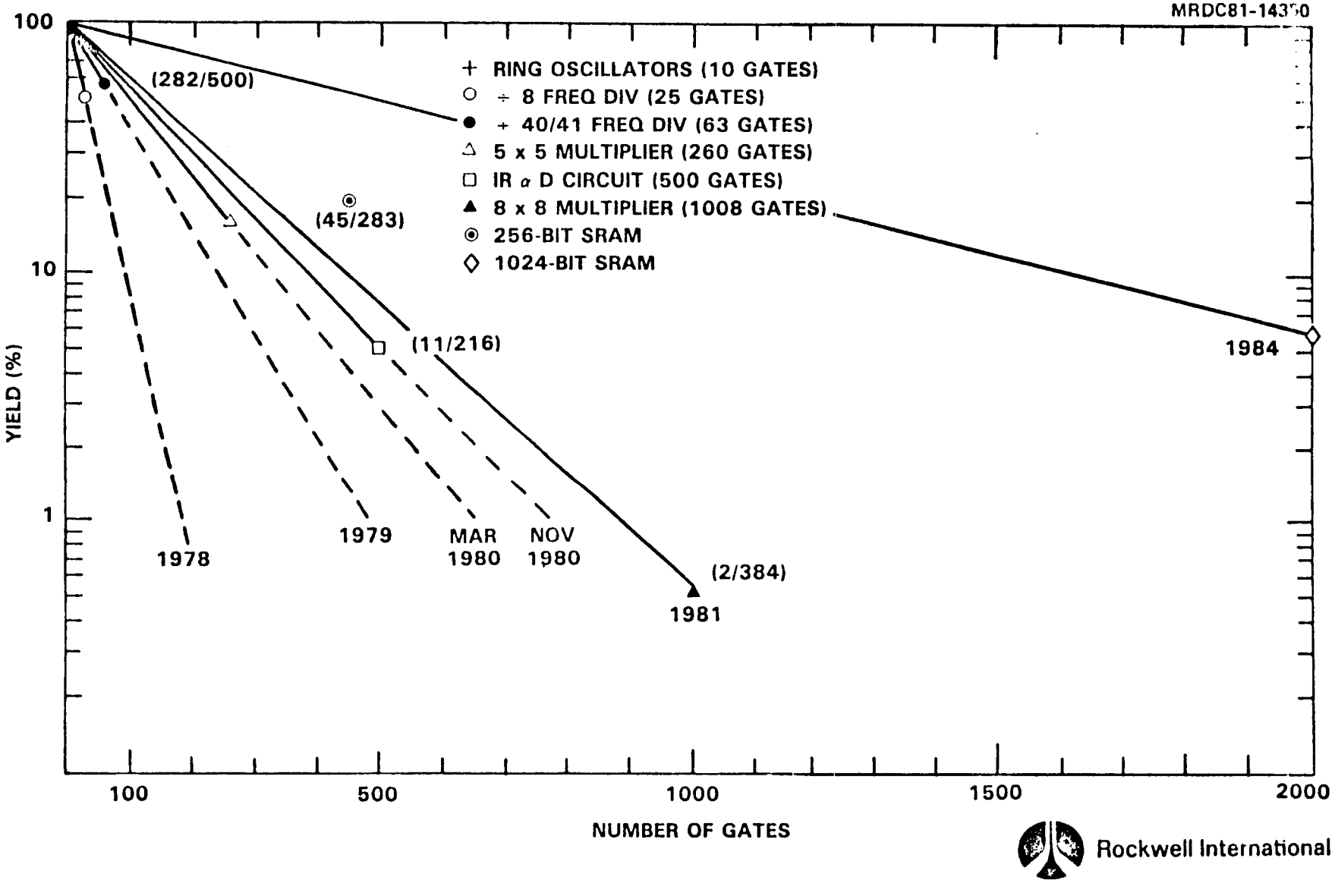
DESIGN CHARACTERISTICS

COMPLEXITY	
8 BIT GENERAL PROCESSOR	950 GATES
GATE ARRAY	437 GATES
CONTROLLER LOGIC	191 GATES
CONTROLLER MICROPROGRAM ROM	744x44 BITS
POWER PER DEVICE	5 WATTS

	8 BIT SLICE (2)	8 BIT SLICE (6)
EXECUTE TIMES		
16 BIT ADD (AIM)	3 CYCLES	3 CYCLES
16 BIT MULTIPLY (MIM)	11	11
32 BIT FLOATING PT. ADD (FAR)	46	5
1750A DIAS INSTRUCTION MIX (5 NSEC CYCLE PERIOD)	12 MIPS	27 MIPS



GaAs IC YIELD vs GATE COMPLEXITY



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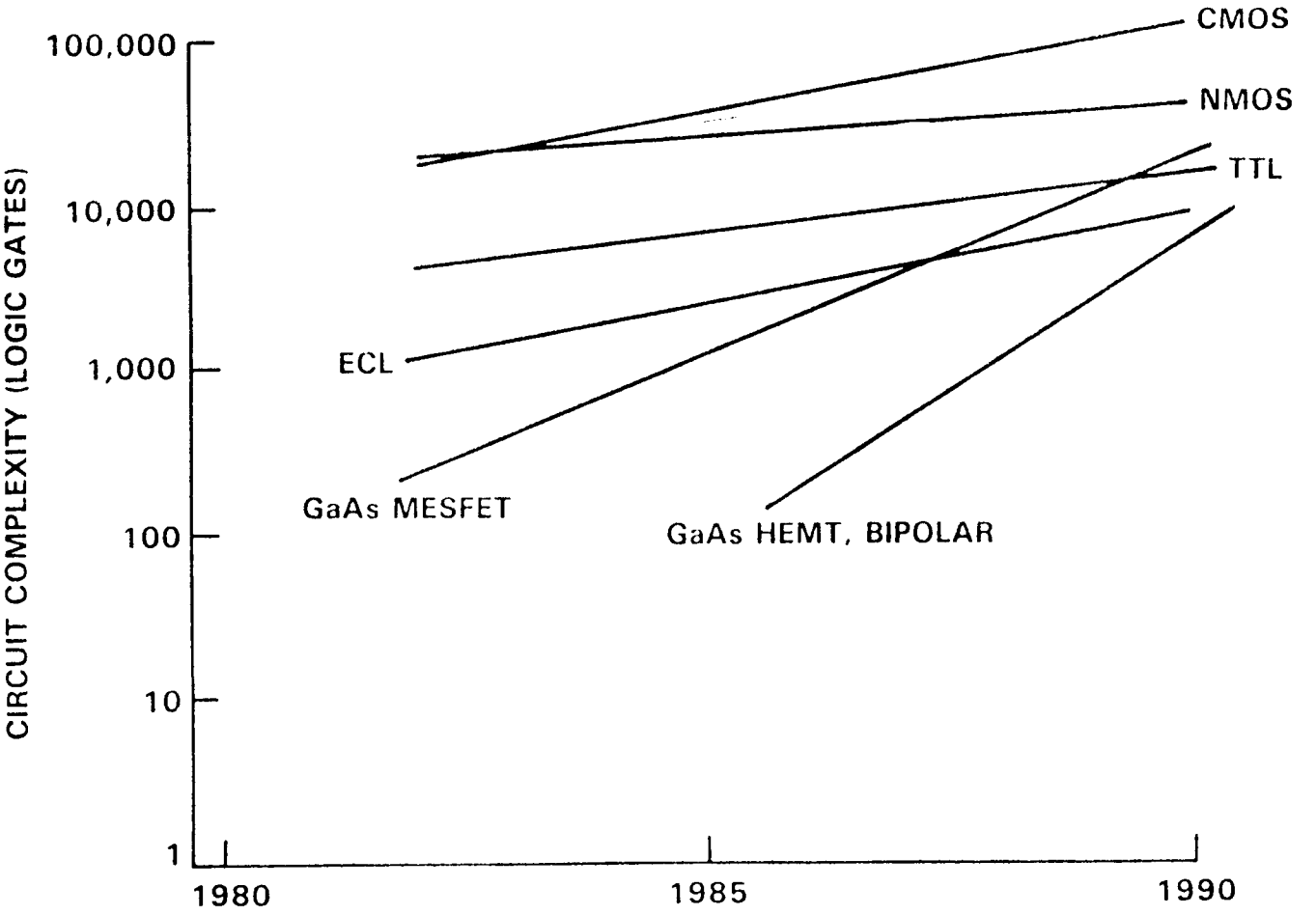
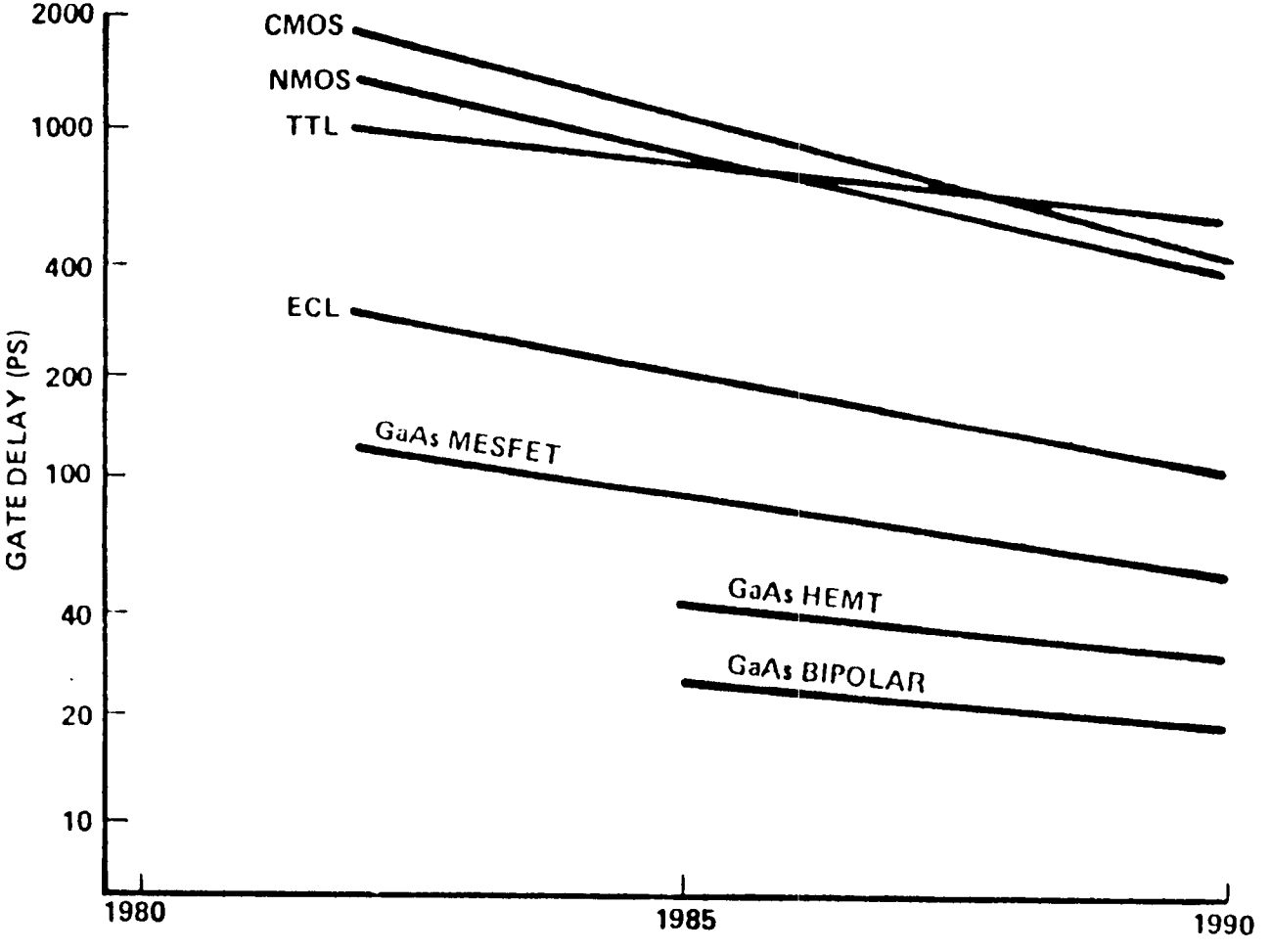
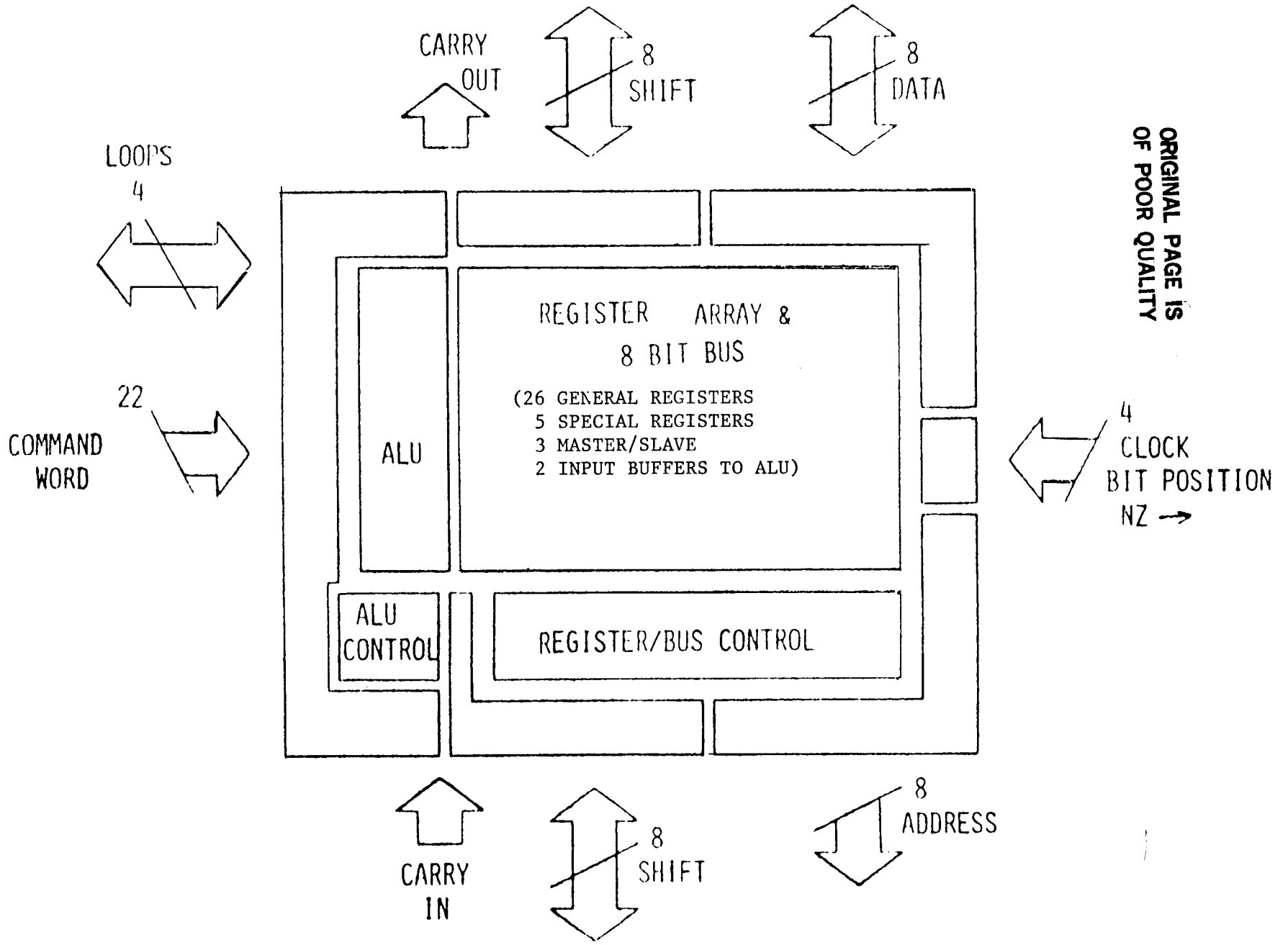
DENSITY COMPARISON OF SILICON AND GaAs INTEGRATED CIRCUITS



SPEED COMPARISON OF SILICON AND GaAs DEVICES





NASA 8-BIT SLICE BLOCK DIAGRAM

ACCOMPLISHMENTS FY84

CONTRACT AWARD FOR GaAs APP CHIP SET	2/84
CHIP SET ARCHITECTURE	11/84

PLANNED ACCOMPLISHMENTS FY85

BIT SLICE/DESIGN PDR (COMPLETED)	2/85
BIT SLICE/GATE ARRAY #1 CDR	6/85
FAB. BIT SLICE/GATE ARRAY	12/85

PLANS

CONTROLLER/GATE ARRAY 2&3 FAB.	8/86
CHIP SET CIRCUIT TESTING	10/86
CIRCUIT BOARD FAB.	4/87
APP CHIP SET SYSTEM TEST	2/88
APP CHIP SET/HEMT TECHNOLOGY	6/89
SELECTED INSTRUCTION SET PROCESSOR (SISP)	2/90

ROCKWELL'S GaAs DIGITAL IC R&D PROGRAMS

MRDC82-19036